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High Efficiency Solution Processed Sintered CdTe Nanocrystal Solar Cells: The Role of Interfaces

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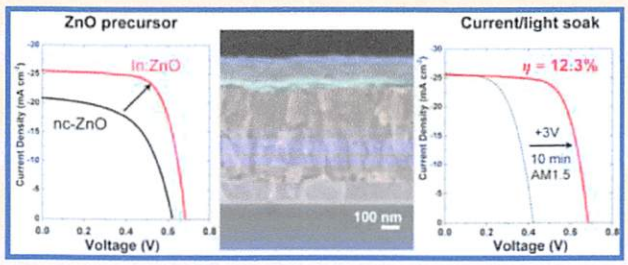
Supporting Information

ABSTRACT: Solution processing of photovoltaic semiconducting layers offers the potential for drastic cost reduction through improved materials utilization and high device throughput. One compelling solution-based processing strategy utilizes semiconductor layers produced by sintering nanocrystals into large-grain semiconductors at relatively low temperatures. Using n-ZnO/p-CdTe as a model system, we fabricate sintered CdTe nanocrystal solar cells processed at 350 °C with power conversion efficiencies (PCE) as high as 12.3%. J_{SC} of over 25 mA cm^{-2} are achieved, which are comparable or higher than those achieved using traditional, close-space sublimated CdTe. We find that the V_{OC} can be substantially increased by applying forward bias for short periods of time. Capacitance measurements as well as intensity- and temperature-dependent analysis indicate that the increased V_{OC} is likely due to relaxation of an energetic barrier at the ITO/CdTe interface.



KEYWORDS: *Nanocrystals, photovoltaics, CdTe, sintering, optoelectronic materials*

Over the past two decades, a number of promising solution-based routes for fabricating semiconductor absorbers for photovoltaics have been developed: dye-sensitized mesoporous TiO_2,[1] organic bulk heterojunctions,[2] colloidal quantum dots,[3−7] hydrazine-based molecular complexes,[8−12] and sintered nanocrystals.[13−17] Colloidal semiconductor nanocrystals have numerous advantages in processing: they are synthesized with high chemical yield, provide materials with controlled stoichiometry, and can sinter easily due to melting point depression.[18] This route produces large-grained films suitable for PV devices with high efficiency and excellent operational stability, unlike some of the aforementioned strategies that may have chemical or thermal stability issues. Recent advancements in surface chemistry have provided an impressive amount of control over the electronic, optoelectronic, magnetic, and catalytic properties of nanocrystal-based films.[19−23] Photovoltaic devices employing sintered nanocrystals have been made using CdTe,[14,24] $Cu(In,Ga)(SeS)_2$,[17] $Cu(In,Ga)Se_2$,[4,25−27] $Cu_2ZnSn(SeS)_4$,[16] and $CuZnGe(SeS)_4$ nanocrystals.[15] Of these, CdTe has advantages in that it is a less complex compound and can be processed in air rather than a chalcogen−vapor environment for sintering to occur.

Seminal work by Gur et al. demonstrated the first all-inorganic nanocrystal-based PV utilizing a sintered CdSe/CdTe bilayer with power conversion efficiency (PCE) approaching 3%.[13] This approach was improved upon to 5.0% by Olson and co-workers who used a Schottky-diode structure.[24] Mulvaney et al. improved this further by depositing the absorber layer in a layer-by-layer approach and using a heterojunction architecture, yielding power conversion efficiencies of over 7% in a CdTe/ZnO heterojuction cell.[14,28]

Here, we fabricated solar cells with sintered CdTe nanocrystals deposited in a layer-by-layer method to prepare a thick (500−600 nm) sintered absorber film in a method similar to that described by Jasieniak and co-workers.[14] We formed a heterojunction using two different ZnO precursors: ZnO nanocrystals and a sol−gel ZnO.[29,30] Through optimized processing of the CdTe absorber and ZnO n-type layer, we attained NREL-certified power conversion efficiencies (PCE) of 8.54%, which could be increased to 12.3% by applying a forward bias current/light soak. We measure short circuit current density (J_{SC}) of over 25 mA cm^{-2} in optimized devices with film thicknesses less than 600 nm. We also obtain excellent fill factor (FF) values of up to 0.72, owing to the excellent film quality and low series resistance.

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We focus on a device structure using commercially available glass/ITO substrates and sequentially deposited 8−12 layers of CdTe via spincoating (resulting in 500−600 nm of total thickness), followed by a ZnO layer prepared in two different methods before thermally evaporating an Al back contact (~8 mm^2) as shown in Figure 1a (see Supporting Information for experimental details). The nanocrystal size was determined to be ~6 nm, measured by the exciton peak position (Figure S1). Each CdTe layer was deposited (on a 25 × 25 mm ITO-coated glass substrate, Thin Film Devices, Inc.) at 800 rpm using colloidal nanocrystals dispersed in a 2:1 1-propanol/pyridine mixture at a concentration of ~40 mg mL^{-1}. After depositing each layer, the substrate was dipped into a saturated solution of $CdCl_2$ in methanol (~15 mg mL^{-1} heated at ~60 °C) for 15 s, immediately rinsed by dipping into a beaker of isopropanol, dried with a stream of N_2 then placed on a 350 °C Al block for 20 s. The substrate was then placed onto an Al block at room temperature to rapidly cool the film. All deposition steps were performed in air inside a fume hood. The use of thin (~50 nm each) layers leads to higher film quality, uniformity, and large columnar grains spanning between the ITO and ZnO layers as shown in the cross-sectional SEM image in Figure 1b. (Additional SEM images are shown in Supporting Information, Figure S2.) This indicates that although the CdTe is deposited in a layer-by-layer fashion, the film recrystallizes after annealing each layer. This is in contrast to previous reports of sintered CdTe nanocrystal solar cells demonstrating that layer-by-layer processing results in grain sizes that were on par with the individual layer thickness.[14] The cause of the larger grain size in our samples is unclear, but we speculate that using very thin layers during processing promotes recrystallization of the entire film, whereas using thicker (~100 nm) layers promotes local densification without recrystallization of the underlying layers. We find that annealing times longer than 30 s or temperatures of 375 °C or higher leads to a reduction in shunt resistance and device yield from shorted devices. Figure 1c,d shows typical *JV* characteristics and external quantum efficiency (EQE) spectra of devices prepared with ZnO layers based on colloidal nanocrystal (nc-ZnO) or sol−gel precursors. The absence of a CdS layer between the window and CdTe results in high quantum efficiency in the 350−500 nm spectral region where conventionally produced CdTe cells do not efficiently convert photons. Devices prepared using the sol−gel precursor exhibit increased J_{SC}, open circuit voltage (V_{OC}), and FF. The sol−gel precursor has two advantages over the nc-ZnO: (1) it produces a smoother and more conformal layer, and (2) it can be easily doped with In to increase the conductivity (see Supporting Information for details). This resulted in a 3-fold decrease in device series resistance, which improved the FF by over 40%. The superior interface created using the sol−gel ZnO likely enhances carrier collection, resulting in the apparent increase in J_{SC} and EQE. Using sol−gel In:ZnO, we achieve J_{SC} values over 25 mA cm^{-2}, FF as high as 0.72, and V_{OC} of up to 685 mV. The device characteristics of cells made with the different ZnO precursors are shown in Table 1. Our best devices have power conversion efficiencies of 12.3%, with typical efficiencies between 11 and 12%.

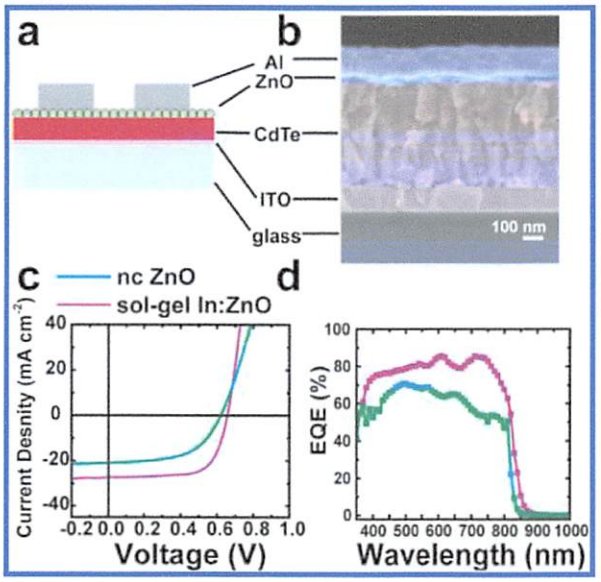

Figure 1. Schematic (a) and cross-sectional SEM (b) of a superstrate style device with the following structure: glass/ITO/CdTe/ZnO/Al (false color added for clarity). *JV* characteristics (c) and external quantum efficiency (d) of devices prepared with colloidal nanocrystal-based ZnO (green) and sol−gel In-doped ZnO (In:ZnO; purple).

Table 1. Device Characteristics and Series Resistance (R_S) of Best Performing Solar Cells Fabricated with Different ZnO layers

	J_{SC} (mA cm^{-2})	V_{OC} (mV)	FF	PCE (%)	R_S (Ω cm^2)
nc-ZnO	20.8	621	0.56	7.3	2.8
sol−gel In:ZnO	25.8	684	0.71	12.3	0.9

As-prepared devices exhibit low V_{OC}'s, ranging from 50 to 450 mV, with typical values around 250 mV. We found that by applying a forward bias (2−3 V) while under illumination (current/light soaking) increases the V_{OC} to 640−690 mV, as shown in Figure 2a. This is typically accompanied by a small (~5−10%) increase in J_{SC} and substantial increase in FF. The combined effect increases the overall PCE from ~2.5% to 11−12%, with best devices reaching 12.3%. Before the current/light soak, the *JV* curve exhibits a rollover in forward bias (Supporting Information, Figure S3), indicative of an energetic barrier at a semiconductor/electrode interface. After the current/light soak, the rollover in forward bias goes away.

We fabricated a series of devices using alternative device structures. A Schottky device was constructed by evaporating a 100 nm thick Al layer directly onto the CdTe. The initial devices typically had very low V_{OC} (<50 mV). Current soaking had a similar effect on this device. Overall PCE was lower (typical 8−9%; highest 9.2%) owing to lower J_{SC}, V_{OC}, and FF. The surprisingly high V_{OC} in the Schottky cell can be attributed to the high barrier height that exists between Al (work function ≈ −4.2 eV) and p-CdTe (E_F ≈ −5.5 eV). We constructed a CdS heterojunction (Figure 2c) device by depositing a ~20 nm CdS layer grown by a modified chemical bath deposition[31] in place of the ZnO as well as an inverted heterojunction (Figure 2d) where the CdS was grown directly onto the ITO in a traditional configuration (details of CdS deposition can be found in the Supporting Information). In the inverted heterojunction cell, ohmic contact was made by thermally evaporating MoO_x (10 nm) followed by 100 nm of Ag. This structure is most similar to what is used in conventional CdTe cells, except back contacts are typically formed by creating a

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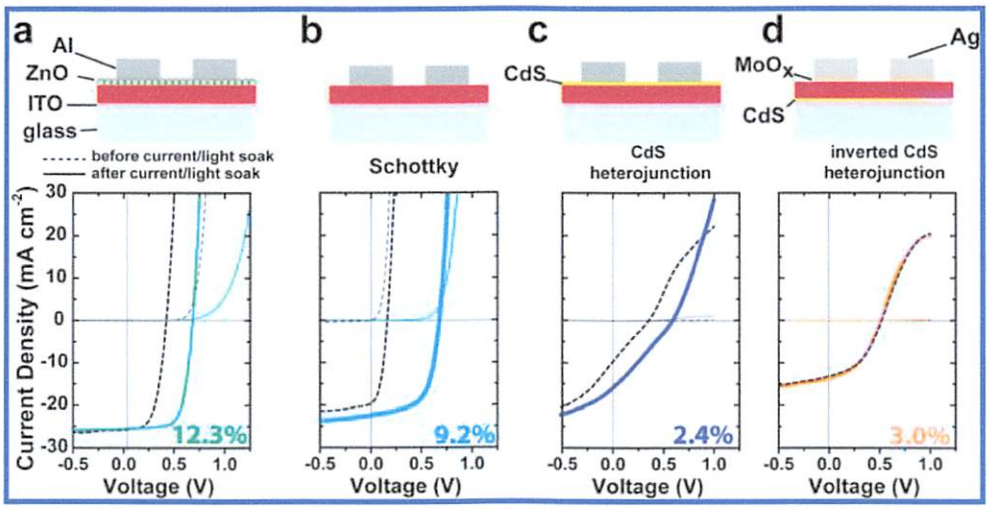

Figure 2. Schematics and *JV* characteristics of different device structures explored in this study. (a) ITO/CdTe/In:ZnO/Al, (b) Schottky structure (ITO/CdTe/Al), (c) CdS heterojunction (ITO/CdTe/CdS/Al), and (d) inverted CdS heterojunction (ITO/CdS/CdTe/Al). *JV* curves in dashed and solid lines correspond to before and after current/light soaking, respectively. The PCE obtained for each structure is noted.

highly doped p+ region via wet etching of the CdTe back surface to create Te-rich regions using dilute bromine/methanol[32] or phosphoric/nitric (NP etch).[33−35] Our attempts to create a p+ interfacial layer by wet etching resulted in either digestion of the CdTe thin film or devices that exhibited diode behavior but no photocurrent. Current/light soaking improved the V_{OC} of the CdS heterojuction (Figure 2c) but not the inverted heterojunction cell (Figure 2d). Because the polarity of the inverted heterojunction is reversed compared to the other cells in this study, we also attempted current/light soaking at −3 V for 10 min, which also had no effect on the J_{SC} or V_{OC}. Device fabricated using CdS as the n-type layer generally had lower PCE, around 2−3% due to lower J_{SC} and V_{OC}. We did not go through extensive optimization for these structures and there may be room for further improvement.

Compositional analysis of CdTe devices and films was obtained using X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) depth profiles (Figure 3). The XPS profile shows sharp interfaces between the ZnO, CdTe, and ITO layers (Figure 3a). XPS at and near the surface of the device showed that the surface has a large atomic percent (0.2%) Cu (Supporting Information, Figure S4). Cu accumulation at contacts is a common occurrence in CdTe devices.[36] The SIMS profile also shows a large (~2 × 10^{18} cm^{-3}) concentration of Cu throughout the CdTe layer. In comparison, Cu concentrations of ~5 × 10^{17} cm^{-3} are observed in SIMS profiles of highly efficient CdTe devices; however, our devices have no intentional copper incorporation during device fabrication.[36,37] To determine whether Cu was introduced during the $CdCl_2$ treatment step, we obtained a SIMS profile of a CdTe film that was deposited onto ITO without the $CdCl_2$ treatment steps during fabrication. Additionally, no ZnO layer was deposited onto this film to eliminate the possibility of impure ZnO precursor being the Cu source. There is a slightly smaller concentration of Cu compared to the $CdCl_2$ treated sample, which can be attributed to the high porosity of the untreated film (which thus has lower concentrations of Cd and Te as well), but no appreciable reduction from omitting the $CdCl_2$ treatment. Therefore, we speculate that Cu is an impurity in reasonably high concentration (several ppm) originating during the synthesis of CdTe NCs, likely from a

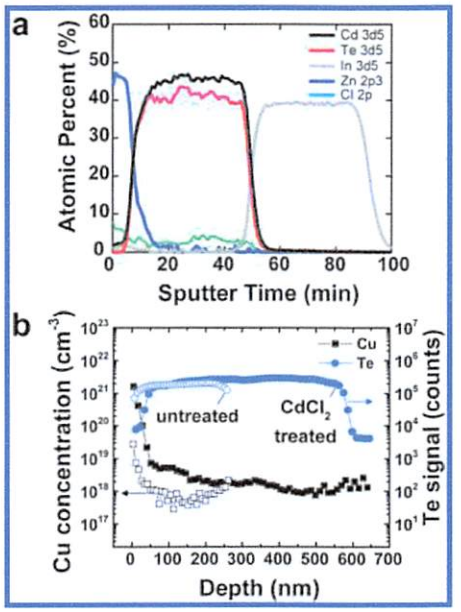

Figure 3. Depth profiling using XPS (a) and SIMS (b). The XPS data and $CdCl_2$-treated SIMS samples (panel b, blue and black) were obtained from In:ZnO/CdTe/ITO stacks, while the untreated sample (panel b, open squares/circles) did not have a ZnO layer deposited to rule out In:ZnO film as the Cu source. The SIMS Te counts (circles) are shown as a guide to show the location of the interfaces.

precursor material, such as CdO. Cadmium is typically obtained from zinc ore, which also contains Cu,[38] so it is reasonable to expect that commercially available Cd compounds could have a substantial Cu content. This finding brings up an important issue of presence of Cu in as-synthesized Cd-chalcogenide NCs.

We used light intensity-dependent current−voltage (*IV*) measurements (Figure 4a) to determine whether the increase in V_{OC} with current/light soaking arises from a change in the trapping mechanism. Ideally, I_{SC} would be linearly proportional to illumination intensity; however, if trap states are filled at low light intensity, there should be a superlinear dependence of $\log(I_{SC})$ with log(intensity) (slope > 1).[39] We found that the

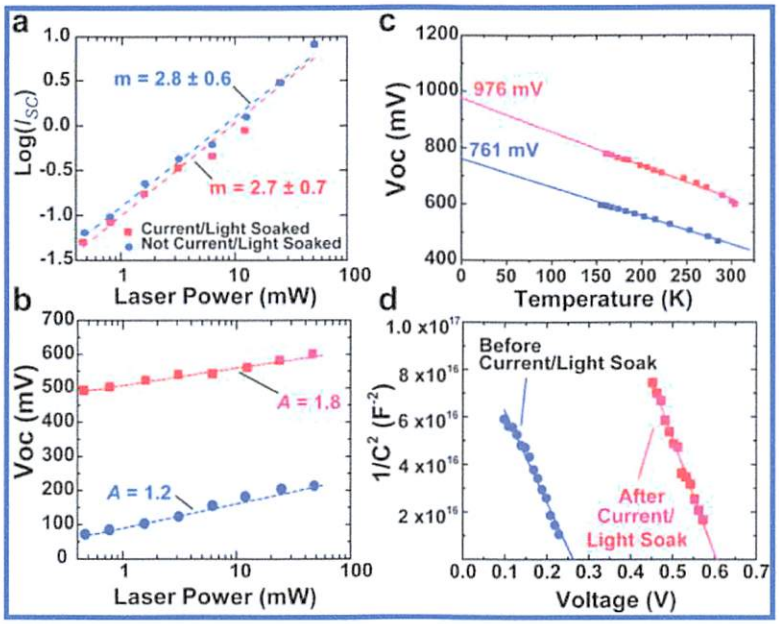

Figure 4. (a) I_{SC} and (b) V_{OC} as a function of illumination intensity (514 nm laser), (c) temperature dependence of V_{OC}, and (d) Mott–Schottky analysis of a ITO/CdTe/Al solar cell. All graphs show data before (blue circles) and after (red squares) current/light soaking. The ideality factor (A) in panel (b) increases from 1.2 to 1.8 with current/light soaking. The slope of the Mott–Schottky plot gives $N_A = 5 \pm 2 \times 10^{15}$ cm^{-3} before and $6 \pm 1 \times 10^{15}$ cm^{-3} after current/light soaking.

intensity-dependent short circuit current (I_{SC}) exhibits super-linear behavior with no significant change in slope (2.8 ± 0.6 to 2.7 ± 0.7) with current/light soaking. These results imply no change in the trap density or depth is occurring within the CdTe during the current/light soak.

We can gain insight into the mechanism of carrier recombination by comparing ideality factors, determined from the intensity-dependence of the V_{OC}:[40]

$$V_{OC} = \frac{E_G}{q} - \frac{Ak_BT}{q}\ln\left[\frac{J_0}{J_L}\right] \quad (1)$$

where E_G is the band gap energy of the absorber layer, A is the diode ideality factor, J_0 is the reverse saturation current, T is temperature, and J_L is the photogenerated current. In our CdTe thin films, J_L is directly proportional to the laser intensity, as nearly 100% of the light from the laser (514 nm) will be absorbed and the exciton dissociation probability is unity.[41] If deep traps within the CdTe dominate charge transport, carrier recombination is dictated by the presence of both holes and electrons, yielding an ideality factor of 2. If recombination is limited by only the minority carrier concentration the ideality factor should be 1. This latter scenario would indicate either band-to-band recombination within the absorber or interfacial recombination at the absorber–electrode interface. A difference in the ideality factor thus provides some insight into the primary mechanism by which recombination occurs. From the intensity dependence of the V_{OC} (Figure 4b), we observe an increase in ideality factor from 1.2 to 1.8 upon current/light soaking. Considering that the V_{OC}, J_{SC}, and rollover in forward bias all improve after current/light soaking, it can be implied that the ideality factor of 1.2 means that carrier recombination predominantly occurs at an absorber/electrode interface. The increase in ideality factor upon current/light soaking indicates that trap-assisted Shockley–Read–Hall (SRH) recombination plays a larger role in the V_{OC} due to some passivating effect at an interface. To further clarify this, we measured the temperature-dependence of the V_{OC} (Figure 4c). Using eq 1, we see that as $T \rightarrow 0$ K, the V_{OC} should approach E_g/q.[40] The extrapolation of the V_{OC} to 0 K falls well below the bandgap of CdTe ($E_g \approx 1.45$ eV) both before and after current/light soaking, indicating that interfaces limit the V_{OC}, rather than SRH recombination in the CdTe. Furthermore, the 0 K intercept shifts to a higher potential, but still below E_g, after current/light soaking, indicating that this process reduces an interfacial energetic barrier but does not remove it. From the combined intensity/temperature *IV* characterization results we can infer that the V_{OC} is limited by a combination of interfacial effects and SRH recombination within the CdTe and that current/light soaking electronically passivates an interface, increasing the V_{OC}. Upon current/light soaking, the interfacial barrier is reduced and plays less of a role compared to SRH recombination resulting in an increase in A. However, the temperature-dependent V_{OC} data indicates that an interfacial barrier still exists, and addressing this could further improve the V_{OC}.

To help determine whether current/light soaking induces any changes in doping within the CdTe layer, we used Mott–Schottky analysis to determine the acceptor concentration (N_A). For this experiment, the Schottky-structure illustrated in Figure 2b was used rather than a heterojunction, as this structure has a less complicated equivalent circuit and is more straightforward to analyze. The Mott–Schottky plot shows a clear shift in the built-in potential (x-intercept) from 281 to 629 mV with current/light soaking (Figure 4a). This is in good agreement with the crossing point of the intensity-dependent *IV* curves before and after current soaking (Supporting Information, Figure S5). The carrier concentration (N_A) calculated from the slope of C^{-2} vs V did not change significantly with current light soaking ($N_A = 5 \pm 2 \times 10^{15}$ cm^{-3} before and $6 \pm 1 \times 10^{15}$ cm^{-3} afterward). These values are 1 order of magnitude higher than doping densities observed

in typical close-space sublimated (CSS)-deposited CdTe ($\sim 10^{14}$ cm^{-3}).[42] The doping density leads to an equilibrium depletion width of ~400 nm. This is in accordance with the findings of Jasieniak et al.,[14] who found that their solution-processed CdTe solar cells were fully depleted with an ideal CdTe thickness of ~400 nm. In our case, the CdTe is not fully depleted and transport in the remaining ~150 nm must occur via diffusion. The apparent increased diffusion length in our films likely arises from the larger grain size, to which we attribute the higher J_{SC} and PCE values reported here.

The intensity- and temperature-dependent *IV* characteristics along with capacitance−voltage measurements provide a consistent story: current/light soaking does not significantly alter the electronic states within the CdTe (neither trapping nor dopants), but affects rather an interface. On the basis of the observation that the current/light soak only affects devices that have an ITO/CdTe interface, we can infer that an energetic barrier is being reduced at this interface. This energetic barrier could be a result of poor energetic alignment between ITO and CdTe, perhaps Fermi pinning, which is partially rectified upon current/light soaking. We currently hypothesize that this effect could be related to Cu migration. Similar reversible changes in V_{OC} have been reported during accelerated testing conditions, where devices are held under bias while under illumination and have been attributed to Cu migration.[36] These effects occurred on the time scale of days or weeks (compared to ~10 min in our case), but are used on much thicker films and may have substantially lower Cu concentrations. The SIMS and XPS data shown in Figure 3 indicate that Cu tends to migrate toward the CdTe/ZnO interface, and perhaps the current soaking drives Cu ions toward the CdTe/ITO interface. This suggests that controlling the Cu content within the CdTe could further elucidate the cause of the current/light soaking effect and perhaps provide a pathway toward devices that do not exhibit undesirable transient behavior.

The steady-state V_{OC} in the CdTe/In:ZnO heterojunction cells decays slowly over the course of several days to weeks to its original value if stored in the dark and more slowly under continuous illumination. We periodically tested a device held under constant AM1.5 illumination over the course of a day (Figure 5) after current/light soaking (+3 V, 10 min). The device initially had a PCE of 11.8%, V_{OC} of 675 mV, and J_{SC} of ~25 mA. The V_{OC} dropped by around 10% in the first hour, but only ~15% over 24 h. The drop in V_{OC} was accompanied by a small (less than 10%) decrease in FF. The J_{SC} did not change substantially over 24 h. Subsequent current/light soaking returned the cell's V_{OC} to its high value.

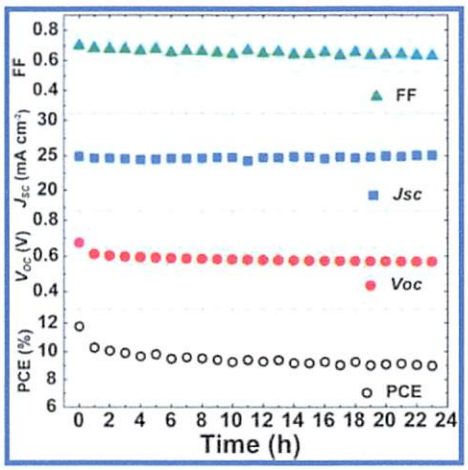

Figure 5. Device performance under constant illumination for 24 h measured in air. *IV* characteristics are taken every 60 min to evaluate the J_{SC}, V_{OC}, FF, and PCE.

After storing a similar device in air for two days and performing a current/light soak, it was submitted to the National Renewable Energy Laboratory's Measurements and Characterization group for testing, showing PCE of 8.54% (Supporting Information, Figure S6). This lower efficiency can be attributed to decline in V_{OC} over time after current/light soaking, as well as contact oxidation, which reduced the J_{SC} and FF.

In summary, we fabricated efficient solar cells using sintered CdTe nanocrystals. Using optimized deposition methods, we fabricated CdTe thin films with columnar grains greater than 500 nm in height. Using a ~50 nm thick sol−gel ZnO doped with 1% In, we achieved power conversion efficiencies of up to 12.3%. The highest J_{SC} values we measured were over 25 mA cm^{-2}, which is comparable to best CdTe solar cells that typically have J_{SC} values around 25−26 mA cm^{-2}.[43] This is achieved despite using a ~550 thick CdTe absorber, compared to 3−5 μm for conventional CSS-deposited CdTe. Using films thicker than ~550 nm did not improve the J_{SC} but typically caused poorer performance due to higher R_S and reduced FF. Our high efficiencies were attained after holding the cell under forward bias (+2 to 3 V) for around 10 min under AM1.5 illumination. This effect appears to be related to altered energetic alignment, at the CdTe/ITO interface rather than electronic changes within the CdTe absorber, such as a change in doping or trap filling. Even after current/light soaking, the temperature dependence of the V_{OC} still has an intercept that is over 400 mV below the bandgap of CdTe. This implies that if an appropriate ohmic contact were found for the CdTe absorber, the V_{OC} should be stable and substantially higher, with even greater PCE. The high doping level achieved ($N_A \approx 5 \times 10^{15}$ cm^{-3}) also shows promise, as it is often difficult to achieve acceptor concentrations greater than 10^{15} cm^{-3} in CSS-deposited CdTe due to its highly compensating nature.[44] This work also suggests routes to further improve performance and stability by controlling the impurity content (particularly Cu) and improving diffusion length by addressing grain boundary passivation.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Experimental details, additional figures, and methods. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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